IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Tadaaki TANIMOTO, et al

Serial No.: Not Yet Assigned

Filed: On Even Date

For: COMPILER AND LOGIC CIRCUIT DESIGN METHOD

INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR 1.97 & 1.98

April 14, 2005

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In the matter of the above-identified application, applicants are submitting herewith copies of any foreign or publication (i.e. articles) documents. Applicants also submit that copies of any U.S. Patents are not being submitted since these documents can be easily obtained by the United States Patent and Trademark Office as listed in the attached form equivalent to Form PTO-1449 for the Examiner's consideration.

This information disclosure statement is being submitted with the new application.

Although some of the documents listed on the attached form equivalent to Form PTO-1449 are not in the English language, the requirement of 37 CFR 1.98 (a) (3) for a concise explanation of the relevance is satisfied by the attached English language abstracts and/or the discussion of these documents in the specification, for example on page 2.

It is respectfully requested that this information disclosure statement be considered by the Examiner.

Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the deposit account of Mattingly, Stanger, Malur & Brundidge, P.C. Deposit Account No. 50-1417 (Case: TAM-103), and please credit any excess fees to such deposit account.

Respectfully submitted,

Mattingly, Stanger & Malur, Brundidge, P.C.

John R. Mattingly
Registration No. 30,293

JRM/nac

Attachments

JC13 Re●PCT/PTO 14 APR 2005

Form PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DKT. NO. TAM-103	SERIAL NO. 10/531287
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)		APPLICANT T. TANIMOTO, et al.	
		FILING DATE April 14, 2005	GROUP

U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date
AA	6,578,187	6/2003	YASUDA			
AB						
AC						
AD						
AE						
AF						
AG						
AH						
AI						
AJ						
AK						
AL						

FOREIGN PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Country	Class	Subclass	Abstract Yes	Abstract No
AM	10-149382	6/1998	JP			X	
AN	2001-117855	4/2001				X	
AO							
AP							
AQ							
AR							
AS							
AT							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	AP	C-based Synthesis Experiences with a Behavior Synthesizer, "Cyber" Wakabayashi, et al.
	AQ	IEEE Std 1076, 2000 Edition. IEEE Standard VHDL Language Reference Manual.
	AR	Cycle-accurate RTL Modeling with Multi-Cycled and Pipelined Components, July 22, 2004.
	AS	HY-C LRM 1.2 Rev 1.1, Nov. 7, 2004
	AT	Kazutoshi Wakabayashi et al., "Densoyo LSI o Dosa"
	AU	Gosei de Kaihatsu, Kino Sekkei no Kikan ga 1/10 ni Tanshuku", Nikkei Electronics, Nikkei Business Publications, Inc., 12 February , 1996 (12.02.96), No. 6555, pages 147-169
	AV	Kurokawa, H. et al., "C++ Based System Simulator for Pre-Verification of System-on-a-Chip Devices", NEC Research & Development, 07 December, 2000 (07.12.00), Vol. 41, No.3, pages 258-263

Examiner	Date Considered